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10/665,080	09/16/2003	Kyung-Oun Jang	25503/81401	6071

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EXAMINER	
TORRES, JUAN A	
ART UNIT	**PAPER NUMBER**
2611	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/665,080	JANG ET AL.	
	Examiner	Art Unit	
	Juan A. Torres	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7* is/are allowed.

6)☒ Claim(s) *1,5,6 and 8-10* is/are rejected.

7)☒ Claim(s) *2 and 3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 September 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *03/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

The drawings are objected to because:

a) The recitation in figure 1"Vhigh" is improper (see figure 7); it is suggested to be changed to "V_{high}"; the recitation "Vlow" is improper (see figure 7); it is suggested to be changed to "V_{low}"; and

b) The recitation "E[DB]" in figures 9(a) and 9(b) is improper, because is not properly constructed; it is suggested to be changed to "E[dB]".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

The disclosure is objected to because of the following informalities:

a) The recitation "S1-Sn" in paragraphs [0030], [0038], [0039], [0043] is improper (see figure 1); it is suggested to be changed to "S_1-S_n".

b) The recitation "FF1-FFn" in paragraphs [0032], [0033] is improper (see figure 3); it is suggested to be changed to "FF_1-FF_n".

c) The recitation "FFn" in paragraph [0032] is improper (see figure 3); it is suggested to be changed to "FF_n".

d) The recitation "Q1-Qn" in paragraphs [0032], [0033], [0038] is improper (see figure 3); it is suggested to be changed to "Q_1-Q_n".

e) The recitation "QB1-QBn" in paragraphs [0032], [0033], [0037], [0038] is improper (see figure 3); it is suggested to be changed to "QB_1-QB_n".

f) The recitation "FF1-FFn-1" in paragraph [0032] is improper (see figure 3); it is suggested to be changed to "FF_1-FF_{n-1}".

g) The recitation "Q1-Qn-1" in paragraph [0032] is improper (see figure 3); it is suggested to be changed to "Q_1-Q_{n-1}".

h) The recitation "Qn" in paragraph [0032] is improper (see figure 3); it is suggested to be changed to "Q_n".

i) The recitation "TG1-TGn" in paragraphs [0033], [0037] is improper (see figure 3); it is suggested to be changed to "TG_1-TG_n".

j) The recitation "TGB1-TGBn" in paragraphs [0033], [0037] is improper (see figure 3); it is suggested to be changed to "TGB_1-TGB_n".

k) The recitation "S1-S4" in paragraphs [0034], [0037], [0038], [0042] is improper (see figure 1); it is suggested to be changed to "S_1-S_4".

l) The recitation "FF1-FF4" in paragraph [0034] is improper (see figure 3); it is suggested to be changed to "FF_1-FF_4".

m) The recitation "Q1", "Q2" and "Q4" in paragraph [0036] is improper (see figure 3); it is suggested to be changed to "Q_1", "Q_2" and "Q_4" respectively.

n) The recitation "FF1", "FF2" and "FF4" in paragraph [0036] is improper (see figure 3); it is suggested to be changed to "FF_1", "FF_2" and "FF_4" respectively.

o) The recitation "Q1-Q4" in paragraph [0038] is improper (see figure 3); it is suggested to be changed to "Q_1-Q_4".

p) The recitation "QB1-QB4" in paragraph [0038] is improper (see figure 3); it is suggested to be changed to "QB_1-QB_4".

q) The recitation "N1-N15" in paragraph [0041] is improper (see figure 5); it is suggested to be changed to "N_1-N_{15}".

r) The recitation "P1-P15" in paragraph [0041] is improper (see figure 5); it is suggested to be changed to "P_1-P_{15}".

t) The recitation "N1-N8" in paragraph [0041] is improper (see figure 5); it is suggested to be changed to "N_1-N_8".

u) The recitation "P1-P8" in paragraph [0041] is improper (see figure 5); it is suggested to be changed to "P_1-P_8".

v) The recitation "P13" in paragraph [0041] is improper (see figure 5); it is suggested to be changed to "P_{13}".

w) The recitation "P14" in paragraphs [0041], [0042] is improper (see figure 5); it is suggested to be changed to "P_{14}".

x) The recitation "N13" in paragraphs [0041], [0042] is improper (see figure 5); it is suggested to be changed to "N_{13}".

y) The recitation "N14" in paragraph [0041] is improper (see figure 5); it is suggested to be changed to "N_{14}".

v) The recitation "P8" in paragraph [0042] is improper (see figure 5); it is suggested to be changed to "P_8".

w) The recitation "P12" in paragraph [0042] is improper (see figure 5); it is suggested to be changed to "P_{12}".

z) The recitation "P15" in paragraph [0042] is improper (see figure 5); it is suggested to be changed to "P_{15}".

aa) The recitation "N1" in paragraph [0042] is improper (see figure 5); it is suggested to be changed to "N_1".

ab) The recitation "N9" in paragraph [0042] is improper (see figure 5); it is suggested to be changed to "N_9".

ac) The recitation "N15" in paragraph [0042] is improper (see figure 5); it is suggested to be changed to "N_{15}".

ad) The recitation "V1-Vn" in paragraphs [0043], [0044] is improper (see figure 8); it is suggested to be changed to "V_1-V_n".

ae) The recitation "Vhigh" in paragraph [0044] is improper (see figure 7); it is suggested to be changed to "V_{high}".

af) The recitation "Vlow" in paragraph [0044] is improper (see figure 7); it is suggested to be changed to "V_{low}".

ag) The recitation "CLK1-CLKn" in paragraph [0044] is improper (see figure 8); it is suggested to be changed to "CLK_1-CLK_n".

ah) The recitation "As shown in FIG. 5, the voltage control unit (200) includes 24 registers (R) (typically 2 n), 15(=23+22+2+1) NMOS transistors (N1-N15), and 15(=23+22+2+1) PMOS transistors (P1-P15). The registers (R) are coupled in series between a power supply voltage (Vdd) and a ground voltage, and the NMOS transistors (N1-N8) and the PMOS transistors (P1-P8) are alternately coupled to the terminals of the registers (R). The NMOS transistors (N1-N8) and the PMOS transistors (P1-P8) are coupled in parallel to the resistors R, and NMOS transistors (N13, N14) and PMOS transistors (P13, P14) are alternately coupled to nodes of the NMOS transistors (N1-N8) and the PMOS transistors (P1-P8). Also, NMOS and PMOS transistors (N15, P15) are coupled to the nodes of the NMOS and PMOS transistors (N13, P13, N14, P14), respectively" in paragraph [0041] is improper (see figure 5 and add the number inside of the parenthesis); it is suggested to be changed to "As shown in FIG. 5, the voltage control unit (200) includes 16 registers (R) (typically 2 n), 15(=8+4+2+1) NMOS transistors (N1-N15), and 15(=8+4+2+1) PMOS transistors (P1-P15). The registers (R) are coupled in series between a power supply voltage (Vdd) and a ground voltage, and the NMOS transistors (N1-N8) and the PMOS transistors (P1-P8) are alternately coupled to the terminals of the registers (R). The NMOS transistors (N1-N8) and the PMOS transistors (P1-P8) are coupled in parallel to the resistors R, and NMOS

transistors (N13, N14) and PMOS transistors (P13, P14) are alternately coupled to nodes of the NMOS transistors (N1-N8) and the PMOS transistors (P1-P8). Also, NMOS and PMOS transistors (N15, P15) are coupled to the nodes of the NMOS and PMOS transistors (N13, P13, N14, P14), respectively" (emphasis added).

Appropriate correction is required.

Claim Objections

Claims 1-6 are objected to because of the following informalities:

As per claim 1, the recitation in line 1 of claim 1 comprising" is improper (see claims 7 and 8); it is suggested to be changed to "comprising:". Appropriate correction is required.

As per claims 2-6, they are objected because they depend directly or indirectly from claim 1 and claim 1 is objected.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 8-10 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 8, claim 8 is rejected because claim 8 recites the limitation "every cycle of the counter" at the beginning of line 4. There is insufficient antecedent basis for this limitation in the claim.

As per claims 9-10, they are rejected because the depend directly from claim 8 and claim 8 is rejected.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 5, 6, and 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balakrishnan (US 6249876 B1) in view of Greiss (US 5731728 A).

As per claim 1, Balakrishnan discloses an electromagnetic interference cancellation system comprising a control signal generation unit having a counter that counts n-bit signals to output a first output signal of n bits with a count value (figure 1 block 140 column 4 lines 28-39); a voltage control unit that outputs a voltage having a step index level corresponding to the count value of the control signal (figure 1 block 150 column 4 lines 28-39); and an oscillator that generates a clock signal having a frequency corresponding to the voltage outputted from the voltage control unit (figure 1 block 110 column 4 lines 28-39). Balakrishnan doesn't disclose a second output signal having a level that is opposite to the first output signal the control signal generation unit alternately outputs the first and second output signals as control signals according to a cycle of the counter. Greiss discloses a second output signal having a level that is opposite to the first output signal the control signal generation unit alternately outputs the first and second output signals as control signals according to a cycle of the counter

(figure 3 column 3 lines 10-22). Balakrishnan and Greiss are analogous art because they are from the same field of electromagnetic interference reduction. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the system disclosed by Balakrishnan the algorithm disclosed by Greiss. The suggestion/motivation for doing so would have been to reduced EMI spectral density of the clock signal (Greiss abstract).

As per claim 5, Balakrishnan and Greiss disclose claim 1, Balakrishnan also discloses that the voltage control unit generates step index voltage having 2n voltage levels corresponding to the count values, and the step index voltage increases and decreases according to the cycle of the counter (figures 2 and 5 column 5 line 57 to column 6 line 5; and column 7 lines 57-67).

As per claim 6, Balakrishnan and Greiss disclose claim 1, Balakrishnan also discloses that the oscillator receives the voltage of the voltage control unit as a high level voltage, and generates a clock signal having a frequency which is in inverse proportion to a difference between the high level voltage and a reference low level voltage (figure 1 block 110 column 4 lines 40-61 and figure 2 column 5 line 57 to column 6 line 5).

As per claim 8, Balakrishnan discloses a method for canceling electromagnetic interference by generating clock signals having various frequencies in a predetermined range, the method comprising outputting an n-bit signal at every cycle of the counter, the n-bit signal being counted by an n-bit counter (figure 1 block 140 column 4 lines 28-39); generating an output voltage having a step index level which increases or

decreases stepwise according to a count value of the control signal (figure 1 block 150 column 4 lines 28-39); and generating a clock signal having a frequency corresponding to the level of the output voltage (figure 1 block 110 column 4 lines 28-39). Balakrishnan doesn't disclose alternately outputting a reverse signal of the at every cycle of the counter. Greiss discloses alternately outputting a reverse signal of the at every cycle of the counter (figure 3 column 3 lines 10-22). Balakrishnan and Greiss are analogous art because they are from the same field of electromagnetic interference reduction. At the time of the invention, it would have been obvious to a person of ordinary skill in the art to incorporate in the method for canceling electromagnetic interference disclosed by Balakrishnan the clock modulation algorithm disclosed by Greiss. The suggestion/motivation for doing so would have been to reduced EMI spectral density of the clock signal (Greiss abstract).

As per claim 9, Balakrishnan and Greiss disclose claim 8, Balakrishnan also discloses that the level of the output voltage alternately increases and decreases according to the cycle of the counter (figures 2 and 5 column 5 line 57 to column 6 line 5; and column 7 lines 57-67).

As per claim 10, Balakrishnan and Greiss disclose claim 8, Balakrishnan also discloses that the clock signal is generated by an oscillator which receives the output voltage as a high level voltage such that the clock signal has a pulse width proportional to a difference between the high level voltage and a reference low level voltage (figure 1 block 110 column 4 lines 40-61 and figure 2 column 5 line 57 to column 6 line 5).

Allowable Subject Matter

Claims 2-4 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 7 is allowed.

The following is an examiner's statement of reasons for allowance: claim 7 is allowed because the references cited fail to teach, as applicant has, an EMI cancellation system comprising a control signal generation unit comprising a counter having n first flip-flops that respectively output first and second output signals with opposite levels, the n first flip-flops being coupled to each other in series and each first flip-flop reversing outputs at every cycle of the first and second signals of a previous first flip-flop, a second flip-flop that outputs third and fourth output signals having opposite levels and being reversed at every cycle of the first and second output signals of a final first flip-flop of the counter, and a multiplexer for passing the first signals of the n first flip-flops as a control signal of n bits when the third output signal of the second flip-flop is a first level and passing the second output signals of the n first flip-flops as the control signal of n bits when the third output signal of the second flip-flop is a second level, a voltage control unit that outputs voltages having respective step index levels corresponding to count values of n-bit control signals, and an oscillator that generates a clock signal having a frequency corresponding to the step index level of the voltage of the voltage control unit, as the applicant has claimed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Juan A. Torres whose telephone number is 571-272-3119. The examiner can normally be reached on 8-6 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Juan Alberto Torres
01-23-2007